UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,465	04/21/2004	Shai Fultheim	A-10799.COM/cat	5322

20741 7590 05/18/2009

HOFFMAN WASSON & GITLER, P.C
CRYSTAL CENTER 2, SUITE 522
2461 SOUTH CLARK STREET
ARLINGTON, VA 22202-3843

EXAMINER	
SILVER, DAVID	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
05/18/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,465	FULTHEIM ET AL.	
	Examiner	Art Unit	
	DAVID SILVER	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Instant Office Action is in response to a Request for Continued Examination filed 3/17/2009.

2. Claims 1-45 are currently pending in Instant Application.

Response to Arguments

Response: 35 U.S.C. § 102

3. **Examiner Response:**

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection, necessitated by amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-9, 11, 13-23, 25, 27-34, 36-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugnion **(US 6075938 A)** ("Patent" hereinafter) and Bugnion's "Disco: Running Commodity Operating Systems on Scalable Multiprocessors" ("Disco" hereinafter) in view of Nickel **(US 20030005068)**.

Bugnion discloses: 1. A method for executing a software application in a plurality of computers having respective hardware resources said hardware resources comprising a respective memory and a respective I/O device, wherein said computers include a first computer and a second

computer that intercommunicate over a network, said computers being operative to execute a virtual machine that runs under a guest operating system, comprising the steps of:

running at least a first virtual machine implementer and a second virtual machine implementer on said first computer and said second computer using said respective memory **(Disco: Fig 1 and description, section 7 "the techniques it uses also apply to more loosely-coupled environments such as networks of workstations (NOW).")**; and

sharing said virtual machine between said first virtual machine implementer and said second virtual machine implementer using said respective I/O device in each of said first computer and said second computer to intercommunicate between said first computer and said second computer **(Disco: section 4.2.4: "The interposition on all DMA requests offers an opportunity for Disco to share disk and memory resources among virtual machines.; page 2 Fig 1 description: "The multiprocessor consists of a set of processing elements (PE) connected by a high-performance interconnect. Each processing element contains a number of processors and a portion of the memory of the machine."; emphasis by Examiner")**.

Disco however does not expressly teach "wherein said first and second virtual machine implementers run separately and independently of one another on said first and second computers, respectively".

Nickel, however, teaches an analogous system having the said feature **(Fig 1B and 1C; PGPUB para 0009: "building a parallel virtual machine comprising a master computer and at least one slave computer, wherein the at least one slave computer is selected from the plurality of multipurpose computer workstations;"; PGPUB para 0039: "PVM daemon 110 may be any software application for establishing a parallel virtual machine comprising independent**

computer systems working in collaboration.").

Disco already has a multiprocessor system (which contains multiple processors), but does not expressly state that the implementers run separately and independently of one another. In this situation, the hosts (first and second computer) are clearly independent in view of PGPUB para 0171, which recites that the hosts can join and leave the virtual supercomputer.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the references in order to have a faster virtual computer because an entire dedicated computer is faster than just a single core of a multiprocessor. Furthermore, this type of combination would have yielded scalable while is a feature that is sought after in the computer industry.

In view of KSR v. Teleflex Supreme Court ruling, it is asserted that one of ordinary skill in the art could have applied the known technique of using the method of parallel distribution / multiprocessor in the same way to the distributed computers (base device) as the claimed invention and the results would have been predictable.

See MPEP 2145 [R-6], X, B, " [A] person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely that product [was] not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under § 103." KSR International Co. v. Teleflex Inc., 550 U.S. ___, ___, 82 USPQ2d 1385, 1397 (2007).

Bugnion and Nickel discloses: 2. (currently amended) The method according to claim 1, further comprising the step of running said software application over said guest operating system, so that commands invoked by said software application are monitored or emulated by said first virtual machine implementer and said second virtual machine implementer on said first computer and said second computer, while said hardware resources of said first computer and said second

computer are shared by communication over said network **(Disco: section 3.1, subsection titled "Overheads": "Operations such as the execution of privileged instructions [...] [are] [...] emulated in software by the monitor. Similarly, the access to I/O devices is virtualized, so requests must be intercepted and remapped by the monitor.)**.

Bugnion and Nickel discloses: 3. (original) The method according to claim 1, wherein at least one of said first virtual machine implementer and said second virtual machine implementer is a virtual machine monitor **(Disco: section 1 paragraph 3: "This layer acts like a virtual machine monitor in that multiple copies of "commodity" operating systems can be run on a single scalable computer.")**.

Bugnion and Nickel discloses: 4. (original) The method according to claim i, wherein at least one of said first virtual machine implementer and said second virtual machine implementer is an emulator **(Disco: section 4.1 subsection "Processors" paragraph 1: "Disco correctly emulates all instructions, the memory management unit, and the trap architecture of the processor allowing unmodified applications and existing operating systems to run on the virtual machine.")**.

Bugnion and Nickel discloses: 5. (currently amended) The method according to claim 1, wherein at least said first computer comprises a first virtual node comprising a first physical CPU of said first computer and a second virtual node comprising a second physical CPU of said first computer **(Disco: Fig 1 and description, section 7 "the techniques it uses also apply to more loosely-coupled environments such as networks of workstations (NOW)."; Fig 2; section 4 para 1: "consists of a collection of nodes each containing a processor, main memory, and I/O devices.")**.

Bugnion and Nickel discloses: 6. (original) The method according to claim 1, wherein said virtual machine comprises a first virtual machine and a second virtual machine, wherein said first virtual machine and said second virtual machine have a plurality of virtual CPU's that are virtualized by said first virtual machine implementer based on a first physical CPU and said second virtual

machine implementer based on a second physical CPU, respectively **(Disco: Fig 1; section 3 para 1: "This layer of software, called a virtual machine monitor, virtualizes *all the resources of the machine*, exporting a more conventional hardware interface to the operating system. The monitor manages all the resources so that multiple virtual machines can coexist on the same multiprocessor."; section 4.1 subsection "Processors": "To match the FLASH machine, the virtual CPUs of Disco provide the abstraction of a MIPS R10000 processor."; section 4.2.1)**.

Bugnion and Nickel discloses: 7. (original) The method according to claim 6, and a first virtual node comprises said first physical CPU and said second physical CPU **(Fig 1, PEs)**.

Bugnion and Nickel discloses: 8. (original) The method according to claim 7, wherein said first virtual machine implementer virtualizes at least one of said virtual CPU's of said first virtual machine based on said first physical CPU and virtualizes at least one of said virtual CPU's in said second virtual machine based on said second physical CPU **(Disco: Fig 1; section 3 para 1: "This layer of software, called a virtual machine monitor, virtualizes all the resources of the machine, exporting a more conventional hardware interface to the operating system.")**.

Bugnion and Nickel discloses: 9. (currently amended) The method according to claim 1, further comprising the steps of:

> providing a management system for said first virtual machine implementer and said second virtual machine implementer to control said first computer and said second computer node, respectively, wherein said management system comprises a wrapper for receiving calls to a device driver from said first virtual machine implementer, said wrapper invoking said device driver according to a requirement of said first virtual machine implementer **(section3.1 subsection "Overheads" para 1: "Similarly, the access to I/O devices is virtualized, so requests must be intercepted and remapped by the monitor.")**.

Bugnion and Nickel discloses: 11. (currently amended) The method according to claim 9, further comprising the step of providing a virtual DMA controller for said management system to control a physical DMA controller in one of said computers **(section 4.2.4 titled "Virtual I/O Devices" paragraph 2)**.

Bugnion and Nickel discloses: 13. (currently amended) The method according to claim 1, further comprising the steps of:

with said first virtual machine implementer and said second virtual machine implementer maintaining mirrors of a portion of said respective memory that is used by said guest operating system in each of said computers **(section 6.3: "Disco simply mirrors the interface of the raw hardware."; Fig 4 and descriptions; section 3 second to last paragraph)**;

write-invalidating at least a portion of a page of said respective memory in one of said computers **(section 4.2.2 para 3: " The pmap entry also contains backmaps pointing to the virtual addresses that are used to *invalidate* mappings from the TLB when a page is taken away from the virtual machine by the monitor.")**; and transferring a valid copy of said portion of said page to said one computer from another of said computers via said network **(section 4.2.3 paragraph 3: "It first invalidates any TLB entries mapping the old machine page and then copies the data to a local machine page. To replicate a page, the monitor must first downgrade all TLB entries mapping the machine page to ensure read-only accesses. It then copies the page to the local node and updates the relevant TLB entries mapping the old machine page.")**.

As per claims 14-21 note the rejection of claims 1, and 3-8 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Bugnion and Nickel discloses: 22. (currently amended) The computer software product according

to claim 14, wherein said computer is further instructed to perform the step of running said software application over said guest operating system, so that commands invoked by said software application are received said first virtual machine implementer and said second virtual machine implementer on said first computer and said second computer, while said hardware resources of said first computer and said second computer are shared by communication over said network **(section 4.2.6 para 3: "specialized network device"; fig 4 item 1; section 7 para 3: "section 7 "the techniques it uses also apply to more loosely-coupled environments such as networks of workstations (NOW).")**.

As per claims 23, 25, 27 note the rejection of claims 9, and 11, 13 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

As per claims 28, note the rejection of claims 1, 2, 22 above. The Instant Claim recites substantially same limitations as the above-rejected claims and is therefore rejected under same prior-art teachings.

As per claims 29-31, note the rejection of claims 22, 8, 7 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Bugnion and Nickel discloses: 32. (currently amended) The computer system according to claim 31, wherein said first computer comprises a first processor and a second processor, a first I/O device and a second I/O device, wherein said first I/O device is assigned to said first processor, and said second I/O device is assigned to said second processor **(section 3.1 subsection "Overheads": "Similarly, the access to I/O devices is virtualized, so requests must be intercepted and remapped by the monitor."; section 4 para 1: "The FLASH multiprocessor consists of a collection of nodes each containing a processor, main memory, and I/O devices."; section 4.1 subsection titled "I/O Devices", section 4.2.1 para 1)**.

Bugnion and Nickel discloses: 33. (currently amended) The computer system according to claim 28, further comprising a minimal operating system executing in each of said computers nodes to invoke said first virtual machine implementer and said second virtual machine implementer so that said first virtual machine implementer and said second virtual machine implementer control said computers nodes **(Fig 1 item "ThinOS" and description; section 4.4 running a thin OS (minimal OS))**.

As per claims 34, 36-37, note the rejection of claims 9, 11, 13 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Bugnion and Nickel discloses: 38. The method according to claim 1, wherein said guest operating system consists of exactly one instance of a single guest operating system **(Fig 1: element "Disco")**.

As per claims 39, note the rejection of claims 38 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Bugnion and Nickel discloses: 40. The method according to claim 1, wherein said first virtual machine implementer and said second virtual machine implementer are operative to present said respective memory of said first computer and said respective memory of said second computer as a single shared memory to said guest operating system, the method further comprising the step of distributing instructions of said guest operating system to said single shared memory **(Fig 1 description: "The multiprocessor consists of a set of processing elements (PE) connected by a high-performance interconnect. Each processing element contains a number of processors and a portion of the memory of the machine."; emphasis by Examiner; page 4 section 4.1 titled "Physical Memory" - "Disco provides an abstraction of main memory"; section 4.2 "Disco is implemented as a multi-threaded shared memory program")**.

As per claims 41-42, note the rejection of claims 40 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Bugnion and Nickel discloses: 43. (new) The method according to claim i, wherein said first and second computers comprise separate, respective first and second central processing units (CPUs), first and second memories, first and second I/O devices, and first and second buses that respectively interconnect the first CPU with the first I/O device and the second CPU with the second I/O device **(Nickel: PGPUB para 0039; Fig 1C item 120)**.

Bugnion and Nickel discloses: 44. (new) The computer software product according to claim 14, wherein said first and second computers comprise separate, respective first and second central processing units (CPUs), first and second memories, first and second I/O devices, and first and second buses that respectively interconnect the first CPU with the first I/O device and the second CPU with the second I/O device **(Nickel: PGPUB para 0039; Fig 1C item 120)**.

Bugnion and Nickel discloses: 45. (new) The computer system according to claim 28, wherein said first and second computers comprise separate, respective first and second central processing units (CPUs), first and second memories, first and second I/O devices, and first and second buses that respectively interconnect the first CPU with the first I/O device and the second CPU with the second I/O device **(Nickel: PGPUB para 0039; Fig 1C item 120)**.

5. Claims 10, 12, 24, 26, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugnion **(US 6075938 A)** ("Patent" hereinafter) and Bugnion's "Disco: Running Commodity Operating Systems on Scalable Multiprocessors" ("Disco" hereinafter) in view of in view of Nickel **(US 20030005068)** as applied to claim 1 above, and further in view of Official Notice taken.

As per claim 10, Bugnion fully discloses claim 9. Bugnion however does not expressly disclose the step of providing a virtual PCI controller for said management system to control a physical PCI controller in one of said computers. Official Notice is taken with respect to this limitation. It

would have been obvious to one of ordinary skill in the art <computer engineer / simulation / virtual machines / virtual machine monitors> at the time of Applicant's invention to combine the features in order to allow for an extensible platform which can be expanded with PCI cards/adapters; thus, saving money associated with having to rebuild a customized system when expansions are required and no adapters are available. Furthermore, having a virtual PCI controller such that the virtual machines can communicate with the actual machine's PCI controller which are routinely used for, for example, sounds cards, video cards, and other I/O devices. In fact, Bugnion discloses virtualized I/O in section 4.2.4 titled "Virtual I/O Devices".

As per claim 12, Bugnion fully discloses claim 11 and identifying devices having on-board i0 DMA controllers **(section 4.2.2 para 4; section 4.2.4 para 2: "Devices such as disks and network interfaces include a DMA map as part of their arguments. Disco must intercept such DMA requests to translate the physical addresses specified by the operating systems into mac)**. Bugnion however does not expressly disclose providing a virtual PCI controller to control a physical PCI controller in one of said computers; and during a bootup phase of operation scanning a device list. Official Notice is taken with respect to these limitations. The PCI controller limitation has been addressed in claim 10 above. It would have been obvious to perform the scanning during the bootup such that the DMA devices could be instantly usable, rather than wasting time and money associated therewith while the system performs scanning later. Rather, it would be more convenient to have the scanning done while the system is starting up.

As per claims 24, 26, 35, note the rejection of claims 10, 12 above. The Instant Claims recite substantially same limitations as the above-rejected claims and are therefore rejected under same prior-art teachings.

Support for Amendments and Newly Added Claims

Applicants are respectfully requested, in the event of an amendment to claims or submission of new claims, that such claims and their limitations be directly mapped to the specification, which

provides support for the subject matter. This will assist in expediting compact prosecution. MPEP 714.02 recites: "Applicant should also specifically point out the support for any amendments made to the disclosure. See MPEP § 2163.06. An amendment which does not comply with the provisions of 37 CFR 1.121(b), (c), (d), and (h) may be held not fully responsive. See MPEP § 714." **Amendments not pointing to specific support in the disclosure may be deemed as not complying with provisions of 37 C.F.R. 1.131(b), (c), (d), and (h) and therefore held not fully responsive.** Generic statements such as "Applicants believe no new matter has been introduced" may be deemed insufficient.

Requests for Interview

6. In accordance with 37 CFR 1.133(a)(3), requests for interview must be made in advance. Interview requests are to be made by telephone (571-272-8634) call or FAX (571-273-8634). Applicants must provide a detailed agenda as to what will be discussed (generic statement such as "discuss §102 rejection" or "discuss rejections of claims 1-3" may be denied interview). The detail agenda along with any proposed amendments is to be written on a PTOL-413A or a custom form and should be faxed (or emailed, subject to MPEP 713.01.I / MPEP 502.03) to the Examiner at least 3 days prior to the scheduled interview.

7. Interview requests submitted within amendments may be denied because the Examiner was not notified, in advance, of the Applicant Initiated Interview Request and due to time constraints may not be able to review the interview request to prior to the mailing of the next Office Action.

Conclusion

8. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached

on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/ DS /
David Silver, Patent Examiner
Art Unit 2128

/David Silver/
Examiner, Art Unit 2128